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PATENT APPLICATION

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Transmitted herewith for filing is the patent application of:

Inventor or Application Identifier:
Riccardo G. Dorbolo

Entitled: METHOD AND SYSTEM FOR REPROGRAMMING INSTRUCTIONS FOR A SWITCH

Enclosed are:

_X_ Specification (_29__ Total Pages)
_X_ Drawing(s) (__3_Total Sheet(s) of _X_ Formal ___ Informal)
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FEE CALCULATION					FEE
	Number		Number Extra	Rate	Basic Fee
					$ 690.00
Total Claims:	30	-20 =	10	X $18 =	$ 180.00
Independent Claims	6	- 3 =	3	X $78 =	$ 234.00
				TOTAL FILING FEE =	$ 1,104.00

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Respectfully submitted,
BAKER BOTTS L.L.P.
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Riccardo G. Dorbolo
Date Filed: July 31, 2000
Title: METHOD AND SYSTEM FOR REPROGRAMMING INSTRUCTIONS FOR A SWITCH

BOX PATENT APPLICATION

Honorable Assistant Commissioner
For Patents
Washington, D.C. 20231

Dear Sir:

CERTIFICATE OF MAILING BY EXPRESS MAIL

I hereby certify that the attached Application Transmittal Form, Patent Application, executed Declaration and Power of Attorney, three (3) sheets of Formal Drawings, Assignment, Assignment Cover Sheet, firm checks in the amount of $1,104.00 to cover the application filing fee, and $40.00 assignment recordation fee, and this Certificate of Mailing are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on this 31st day of July, 2000 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

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METHOD AND SYSTEM FOR REPROGRAMMING INSTRUCTIONS FOR A SWITCH

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to the field of telecommunication switching, and more particularly to a method and system for reprogramming instructions for a switch.

BACKGROUND OF THE INVENTION

The Internet has dramatically increased the potential for data, voice, and video services for customers. Existing circuit-switched telephony systems, however, do not provide the foundation to support the growing need for bandwidth and new services required by both residential and business consumers. As a result, integrated access devices (IADs) have been introduced to support Internet and related technologies as well as standard telephony service for customers.

IADs often combine synchronous and asynchronous transport and switch functionality to multiplex data, voice, and video traffic together onto a single network. Within an IAD, a time division multiplex (TDM) bus is typically used to transport voice and other synchronous traffic between the line cards and a switch core. An asynchronous transfer mode (ATM) bus is used to transport ATM traffic between the line cards and the switch core.

At the switch core, ATM traffic normally arrives asynchronously while TDM traffic arrives in a regular and periodic fashion. Separate ATM and TDM switch hardware are provided to receive and process the ATM and TDM traffic, respectively.

Typically, the TDM traffic is switched by a synchronous switch such as a time slot interchanger (TSI) that cross-connects the TDM channels based on switching instructions in a switching memory. The switching instructions are preprogrammed into the switching memory by a processor and may be altered by the processor in response to protection switching and other events.

For 1:N protection switching, a standby card in the system is provided to be activated in case one of a

number of designated cards malfunctions. When a defect is detected in an operating card and the standby card is activated in its place, the switching memory for the TSI is reprogrammed to write each instruction for the failed card to the instructions for the activated card. This reprogramming of the switching memory involves a large number of microprocessor operations which are relatively time consuming. As a result, protection switching is slowed down in the TSI and may not conform to some telecommunication standards.

SUMMARY OF THE INVENTION

The present invention provides a method and system for reprogramming instructions or other routing parameters for a time slot interchanger (TSI) or other switch that substantially eliminates or reduces problems and disadvantages associated with previous systems and methods. In particular, each set of routing parameters in a routing memory is selectively associated with a line card in a redirection memory that can be reprogrammed to switch a routing parameter set for a failed line card to a protect line card with minimal processor operations.

In accordance with one embodiment of the present invention, a method and system for reprogramming instructions for a switch includes programming a redirection memory to associate a routing parameter set in a routing memory for the switch with a first line card. The routing parameter set includes a plurality of routing parameters to be provided to the switch to service the first line card. In response to an event initiating activation of a second line card in place of the first line card, the redirection memory is reprogrammed to associate the routing parameter set in the routing memory with the second line card.

More specifically, in accordance with a particular embodiment of the present invention, the routing parameters are instructions, the routing parameter set is an instruction set and the routing memory is an instruction memory for a synchronous switch. In this and other embodiments, the event may be a failure of the first line card. The redirection memory may be initially programmed to associate a second instruction set in the instruction memory with the second line card. The second

instruction set includes a plurality of instructions to be provided to the synchronous switch to service the second line card. In response to the event initiating activation of the second line card in place of the first line card, the redirection memory is reprogrammed to associate the second instruction set with the first line card. In this way, instruction sets are switched between the line cards. The synchronous switch may be a time slot interchanger (TSI) or other suitable switch.

In accordance with one aspect of the present invention, instructions are provided to the synchronous switch by generating a count value including a first portion and a second portion. The second portion is operable to identify a relative location in one of a plurality of instruction sets in an instruction memory for the synchronous switch. The redirection value is determined for the first portion of the count value based on the first portion of the count value. The redirection value identifies an instruction set in the instruction memory. An instruction is read from the relative location in the instruction set based on the redirection value and the second portion of the count value. In a particular embodiment, the count value is a unitary value in which the first portion comprises a set of most significant bits (MSB) of the unitary value and the second portion comprises a set of least significant bits (LSB) of the unitary value.

Technical advantages of the present invention include providing an improved method and system for reprogramming routing parameters for a switch, such instructions for a TSI. In particular, each set of instructions in the instruction memory is selectively

associated with a line card in a programmable redirection memory. The redirection memory may be reprogrammed with minimal processor operations to switch an instruction set of a failed line card to a protect line card. As a result, processor operations and cycles are reduced for protection switching. Thus, protection switching occurs rapidly and within the time required by the telecommunication standards.

Another technical advantage of the present invention includes providing an improved TSI or other suitable switch. In particular, the TSI includes an instruction memory and a redirection memory for associating instruction sets with the line cards serviced by the TSI. The redirection memory adds a level of indirection to the TSI that allows N:1 protection switching reprogramming to be performed with only two processor operations. Accordingly, the TSI operates more efficiently and within telecommunication standards.

Other technical advantages of the present invention will be readily apparent to one skilled in the art from the following figures, description, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of present invention and its advantages, reference is now made to the following description taken in conjunction with the accompanying drawings, wherein like reference numerals represent like parts, in which:

FIGURE 1 is a block diagram illustrating a telecommunications system in accordance with one embodiment of the present invention;

FIGURE 2 is a block diagram illustrating a detailed view of a node in the telecommunications system of FIGURE 1 in accordance with one embodiment of the present invention;

FIGURE 3 is a block diagram illustrating details of the synchronous switch of FIGURE 2 in accordance with one embodiment of the present invention;

FIGURE 4 is a block diagram illustrating a details of the instruction system of FIGURE 3 in accordance with one embodiment of the present invention;

FIGURE 5 is a block diagram illustrating details of the redirection memory of FIGURE 4 in accordance with one embodiment of the present invention; and

FIGURE 6 is a flow diagram illustrating a method for reprogramming instructions for the time slot interchanger (TSI) of FIGURE 3 in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIGURE 1 illustrates a telecommunications system 10 in accordance with one embodiment of the present invention. The telecommunications system 10 transmits voice, data, video, other suitable types of information, and/or a combination of different types of information between source and destination points.

Referring to FIGURE 1, the telecommunications system 10 includes customer premise equipment (CPE) 12 and integrated access devices (IADs) 14 connecting the CPE 12 to a network 16. The IADs 14 communicate voice, data, and/or video traffic between the CPE 12 and the network 16.

The CPE 12 includes standard telephones, modems, computers, dataphones, and other devices capable of generating traffic for transmission in the telecommunications system 10. The CPE 12 is connected to the IADs 14 through a communication link 20. The communication link 20 may be a T1 line, conventional twisted pair cable, fiber optic, or other suitable type of wireline and/or wireless link.

The network 16 may include portions of the Internet, one or more intranets, other wide or local area networks, telephony switches such as a class 5 switch and the like. In a particular embodiment, the network 16 includes backbone routers 18 at its borders for communicating with the IADs 14. In this embodiment, the backbone routers 18 may be Cisco 12000 routers. It will be understood that different types of backbone routers 18 as well as different types of devices capable of directing,

switching, or otherwise routing traffic may be used in connection with the present invention.

FIGURE 2 illustrates details of the IAD 14 in accordance with one embodiment of the present invention. In this embodiment, the IAD 14 is implemented in a card shelf configuration with functionality of the device distributed between discrete cards connected over a backplane. The backplane includes one or more transmission busses connecting line cards and switch cards. It will be understood that other types of access devices and/or nodes may be used in connection with the present invention.

Referring to FIGURE 2, the IAD 14 includes line cards 40, a switch core 44, and a backplane 46. The line cards 40 and switch cards of the switch core 44 each include hardware and software stored in random access memory (RAM), read only memory (ROM), and/or other suitable computer-readable memory for performing switch and other functionality of the cards. The line cards 40 are each a discrete card configured to plug into the backplane 46. Used herein, each means every one of at least a subset of the identified items. The switch core 44 comprises one or more discrete switch cards also configured to plug into the backplane 46.

The line cards 40 include customer line cards 48 and network line cards 50 that communicate traffic with network 16. Each line card 48 and 50 includes one or more external interfaces, or ports, one or more internal interfaces, and a traffic processor. The ports receive ingress traffic from an external line and/or transmit egress traffic received by the internal interfaces from the switch core 44. The internal interfaces transmit

ingress traffic received by the ports from the external links and receive egress traffic from the switch core 44. The internal interfaces communicate with the switch core 44 over the backplane 46. The traffic processor is preferably local to the line card 40 and includes hardware and software for processing telephony voice (DS-0) synchronous transmission signal (STS-N) traffic, integrated services digital network (ISDN) traffic, synchronous optical network (SONET) traffic, synchronous digital hierarchy (SDH), asynchronous transfer mode (ATM), and/or other suitable traffic.

The switch core 44 includes a synchronous switch 52 that performs time division multiplex (TDM) switching and an ATM switch 54 that performs cell-based switching. The synchronous switch 52 provides cross-connection for telephony connections, SONET SPEs, other synchronized traffic, and asynchronous traffic segmented into time slots. The ATM switch 54 switches ATM cell traffic, ATM adaption layer (AAL) cell traffic, and segmented packet traffic. The switch core 44 may also convert traffic between the TDM and ATM realms to establish cross-connection between line cards 40.

The switch core 44 or other suitable element of the IAD 14 may implement protection switching for the device 14. In a particular embodiment, 1:N protection switching is provided in the device. In this embodiment, one or more protect line cards 40 provide protection for a number of active line cards 40. When a defect is detected in an active line card 40, the line card 40 is deactivated and the protect line card 40 activated in its place. As described in more detail below, switching

instructions are modified within the switch core 44 to correspond to the change in status of the line cards 40.

FIGURE 3 illustrates the synchronous switch 52 in accordance with one embodiment of the present invention. In this embodiment, the synchronous switch 52 switches 16 bit traffic based on 36 bit instructions. The 16 bit time slots allows channel associated signaling (CAS) and other overhead and/or superframe information to be transported and switched with the traffic. The 36 bit instructions allow sub-channel traffic to be consolidated, expanded, and switched within the synchronous switch 52. Further details regarding the 16 bit time slots and 36 bit instructions are provided in co-owned U.S. Patent Application Serial No. 09/452,828, entitled Time Slot Interchanger (TSI) and Method for a Telecommunications Node filed December 1, 1999, which is hereby incorporated by reference.

Referring to FIGURE 3, the synchronous switch 52 includes a time slot interchanger (TSI) 80 and an instruction system 82 that provides instruction words to the TSI 80. Based on the instruction words, the TSI 80 performs cross connections between TDM channels of the line cards 40.

The TSI 80 is coupled to the line cards 40 through a time slot bus (TSB), an input TSB timing, synchronization, and protection (TTSP) interface 90 and an output TTSP interface 92. The input TTSP interface 90 includes a serial-to-parallel converter for each line card link and a concentrator 94 that multiplexes together the parallel stream produced by the serial-to-parallel converters. In the illustrated embodiment, the concentrator 94 generates a 16 bit composite stream that

is input into the TSI 80. The TSI 80, in turn, generates a 16 bit output stream that is passed to the output TTSP interface 92. The output TTSP interface 92 includes an expander 96 that de-multiplexes and serializes the TSI 80 output for each line card link. The de-multiplex output is serialized by the serializers for transmission to line cards 40.

The TSI 80 is coupled to an exchange memory 100 through a bank selector 102. The exchange memory 100 includes exchange RAM 0 and exchange RAM 1 between which the TSI 80 alternates each frame cycle. In particular, egress traffic is stored into one of the exchange RAMs each frame while traffic from a previous frame is read out of the other exchange RAM during the frame. The bank selector 102 alternately selects each of the exchange RAMs for receiving ingress traffic written to the exchange memory 100 by the TSI 80 or providing egress traffic read from the exchange memory 100 by the TSI 80.

The instruction system 82 is coupled to the TSI 80 and provides program switching instructions to the TSI 80 in the form of instruction words. The instruction words provides read and write operations for transferring DS-0 and other traffic between time slots of the line cards 40. In this way, the TSI 80 cross-connects TDM channels in the IAD 14.

FIGURE 4 illustrates the instruction system 82 in accordance with one embodiment of the present invention. In this embodiment, the instruction system 82 includes an instruction memory 110, instruction counter 112, redirection memory 114 and a controller 116. It will be understood that the instruction system 82 may include

additional or disparate suitable elements without departing from the scope of the present invention.

Referring to FIGURE 4, the instruction memory 110 is a RAM or other suitable memory or set of memories capable of storing and providing instructions to the TSI 80. The instruction RAM 110 includes an instruction set 120 for each line card 40 of the IAD 14. Each instruction set 120 includes an instruction 122 for each time slot of the associated line card 40. Thus, the instruction set 120 provides cross-connection information for each time slot of the line card 40. In an exemplary embodiment in which the IAD 14 includes 32 line cards that each have 256 time slots per frame, the instruction RAM 110 includes 32 instruction sets 120 that each have 256 instructions for a total of 8,192 instructions. It will be understood that the size and number of the instruction sets 120 may be suitably varied to correspond to the configuration of the IAD 14.

The counter 112 generates an incrementing count value that, as redirected by the redirection memory 114, sets the order of instructions 122 to be read from the instruction RAM 110 by the TSI 80. The count value is incremented linearly during each frame cycle of the TSI 80 from an initial value that absent redirection represents the first instruction 122 in the first instruction set 120 to a final value that absent redirection represents the last instruction 122 of the last instruction set 120. The total count value corresponds to the number of instructions 122 in the instruction RAM 110. In this way, each instruction 122 is read from the instruction RAM 110 to the TSI 80 during each cycle of the TSI 80. In the exemplary embodiment,

the count value is a binary value incremented from zero to 8,191 to read the 8,192 instructions 122 of the instruction RAM 110.

The count value includes a first portion operable to identify the instruction set 120 and a second portion operable to identify the particular instruction 122 in the instruction set 120 to be read. In the exemplary embodiment, the count value is a 12 bit binary value including most significant bits (MSB) 0-4 that identify the instruction set 120 and least significant bits (LSB) 5-11 that identify the location of an instruction 122 relative to an instruction set 120. The MSBs are passed to the redirection memory 114 for redirection in accordance with the current state of the IAD 14 while the LSBs are passed to the instruction RAM 110 to identify an instruction 122 in an instruction set 120 identified by the redirection memory 114 based on the MSBs received from the counter 112. It will be understood that the counter 112 may otherwise suitably identify an instruction set 120 and an instruction 122 and that the count value may be otherwise suitably partitioned for redirection of the instruction set 120 without departing from the scope of the present invention. For example, the counter 112 may include two or more component counters that generate discrete values that together represent the incrementing count value. The counter 112 may be any type of device capable of generating a signal that selects each of the instructions 122 in the instruction RAM 110 in a programmable order.

The redirection memory 114 is a register bank or other suitable type of memory, software, and/or hardware capable of associating an input instruction set 120

identified by the counter 112 with an output instruction set 120 to be read from in the instruction RAM 110, and thus associates each line card 40 with an instruction set 120. The redirection memory 114 adds a level of indirection to the TSI 80. As described in more detail below, the redirection memory 114 allows instruction sets 120 to be selectively associated with the line cards 40 to facility protection switching in the IAD 14 within the time required by telecommunication standards. The redirection register 114 may also allow an instruction set 120 to be associated with a plurality of line cards 40 by listing it as the output instruction sets 120 for the line cards 40. Similarly, instruction sets 120 may be skipped by omitting them in the redirection memory 114.

The controller 116 programs the redirection memory 114 to establish and alter associations between the line cards 40 and the instruction sets 120. The controller 116 may be any suitable type of processor running on program instructions or other logic capable of programming the redirection memory 114 in response to protection switching events within the IAD 14. In one embodiment, the controller 116 may be a processor in the switch core 44 that dynamically programs the redirection memory 114.

FIGURE 5 is a block diagram illustrating the redirection memory 114 in accordance with one embodiment of the present invention. In this embodiment, the redirection memory 114 is implemented as a register bank 130. The redirection register bank 130 includes an input set of registers 132 and an associated output set of registers 134. The input registers 132 include an

identifier for each instruction set 122 in the instruction RAM 110, which corresponds to an instruction set 120 for each line card 40. The input instruction set is used to associate the instruction set identified by the count value with an output instruction set. The output instruction set is programmable by the controller to selectively associate as a unit any instruction set 120 in the instruction RAM 110 with any line card 40.

In operation, the input and output instruction sets in the redirection register bank 130 may be the same when the IAD 14 is under normal operating conditions with no failed line cards 40. In the event of a line card 40 failure and activation of a protect line card 40, the output instruction set 120 for the activated line card 40 is reprogrammed to the instruction set 120 that had been associated with the failed line card 40 to enable the protect line card 40 to perform the instructions, and thus the cross connections for the failed line card 40. Similarly, the output instruction set 120 for the failed line card 40 may be reprogrammed to the instruction set 120 that had been associated with the active line card 40 to allow the failed line card 40 to perform instructions and thus cross connections previously performed by the protect line card 40 to the extent possible. This is typically low priority traffic supported on an as available basis. Reprogramming of the redirection memory 114 may be initiated in response to another suitable event initiating activation of one card in place of another. An action is in response to an event when it is directly or indirectly based on at least the event.

In this way, the TSI 80 is reprogrammed to account for protection switching with only two processor

operations. As a result, protection switching occurs rapidly and within the time required by telecommunication standards. For example, upon failure of line card "2" and activation of protect card "30", activated line card "30" is associated with the output instruction set "2" and the failed line card "2" is associated with output instruction set "30". Thus, when the count value indicates that the instructions 122 for line card "30" are to be read, the redirection memory 114 will instead read the instructions for line card "2". Thus, line card "30" will perform the instruction in place of line card "2".

FIGURE 6 is a flow diagram illustrating a method for conducting protection switching and reprogramming a switch in accordance with one embodiment of the present invention. The switch may be a synchronous switch, packet switch, ATM switch or other suitable switching system including a plurality of line cards, one or more standby or swappable line cards and routing parameters associated with the line cards. The routing parameters are routing tables, instructions, and other information operable to direct traffic in a switching system.

In the illustrated embodiment, the switch is the TSI 80 and a 1:N protection switching is implemented by the IAD 14. It will be understood that other suitable types of protection switching may be implemented in accordance with the present invention.

Referring to FIGURE 6, the method begins at step 150 in which a first instruction set 120 is associated with a first, or working, line card 40. Next, at step 152, a second instruction set 120 is associated with a second, or protect, line card 40. These associations may be made

prior to or during operation of the IAD 14. At step 154, failure of the working line card 40 is detected. Next, at step 156, the protect line card 40 is activated. At step 158, the failed line card 40 is deactivated.

Proceeding to step 160, the output instruction set 120 corresponding to the failed line card 40, or the first instruction set 120 is associated with the input instruction set 120 corresponding to the activated line card 40 in the redirection memory 114. At step 158, the output instruction set 120 corresponding to the activated card 40, or second instruction set 120, is associated with the input instruction set 120 corresponding to the failed line card 40 in the redirection memory 114. Accordingly, the activated line card 40 will perform the instructions in place of the failed line card 40. The failed line card 40 will perform the instructions of the activated line card 40, which may cross connect low priority traffic supported on an as available basis or may be a null set. In this way, protection switching is provided with minimal processor operations and in minimal time.

Although the present invention has been described with several embodiments, various changes and modifications may be suggested to one skilled in the art. It is intended that the present invention encompass such changes and modifications as fall within the scope of the appended claims.

WHAT IS CLAIMED IS:

1. A method for providing instructions to a switch, comprising:

generating a count value including a first portion and a second portion, the second portion operable to identify a relative location in one of a plurality of instruction sets in an instruction memory for a switch;

determining a redirection value for the first portion of the count value based on the first portion of the count value, the redirection value identifying an instruction set in the instruction memory; and

reading an instruction from the relative location in the instruction set based on the redirection value and the second portion of the count value.

2. The method of Claim 1, wherein the first portion of the count value identifies an initial instruction set disparate from the instruction set.

3. The method of Claim 1, wherein the count value is a unitary value and the first portion comprises a set of most significant bits (MSB) of the unitary value and the second portion comprises a set of least significant bits (LSB) of the unitary value.

4. The method of Claim 1, further comprising:

incrementing the count value from an initial value to a final value representing a total number of instructions in the instruction memory, each count value including the first portion and the second portion, the second portion identifying a relative location in one of the instruction sets;

for each count value, determining a redirection value based on the first portion of the count value, the redirection value identifying an instruction set in the instruction memory; and

reading an instruction from the relative location in the instruction set based on the redirection value and the second portion of the count value.

5. The method of Claim 1, wherein the switch is a synchronous switch.

6. The method of Claim 5, wherein the synchronous switch is a time slot interchanger (TSI).

7. A system for providing instructions to a switch, comprising:

a computer-readable medium; and

software stored on the computer-readable medium, the software operable to generate a count value including a first portion and a second portion, the second portion operable to identify a relative location in one of a plurality of instruction sets in an instruction memory for a switch, to determine a redirection value for the first portion of the count value based on the first portion of the count value, the redirection value operable to identify an instruction set in the instruction memory, and to read an instruction from the relative location in the instruction set based on the redirection value and the second portion of the count value.

8. The system of Claim 7, wherein the first portion the count value identifies an initial instruction set disparate from the instruction set.

9. The system of Claim 7, wherein the count value is a unitary value and the first portion comprises a set of most significant bits (MSB) of the unitary value and the second portion comprises a set of least significant bits (LSB) of the unitary value.

10. The system of Claim 7, the software further operable to increment the count value during a cycle of the synchronous switch from an initial value to a final value representing a total number of instructions in the instruction memory, each count value including the first portion and the second portion, the second portion identifying a relative location in one of the instruction sets, to determine for each count value a redirection value based on the first portion of the count value, the redirection value identifying an instruction set in the instruction memory, and to read for each count value an instruction from the relative location in the instruction set based on the redirection value and the second portion of the count value.

11. The system of Claim 7, wherein the switch is a synchronous.

12. The system of Claim 11, wherein the synchronous switch is a time slot interchanger (TSI).

13. A method for associating routing parameters for a switch with line cards serviced by the switch, comprising:

programming a redirection memory to associate a routing parameter set in a routing memory for a switch with a first line card, the routing parameter set including a plurality of routing parameters to be provided to the switch to service the first line card; and

in response to an event initiating activation of a second line card in place of the first line card, reprogramming the redirection memory to associate the routing parameter set in the routing memory with the second line card.

14. The method of Claim 13, wherein the event is a failure of the first line card.

15. The method of Claim 13, further comprising:

programming the redirection memory to associate a second routing set in the routing memory with the second line card, the second routing parameter set including a plurality of routing parameters to be provided to the switch to service the second line card; and

in response to the event initiating activation of the second line card in place of the first line card, reprogramming the redirection memory to associate the second routing parameter set with the first line card.

16, The method of Claim 13, wherein the routing parameters comprise instructions, the routing parameter set comprises an instruction set and the routing memory comprises an instruction memory.

17. The method of Claim 16, wherein the switch comprises a synchronous switch.

18. The method of Claim 17, wherein the synchronous switch is a time slot interchanger (TSI).

19. The method of Claim 13, wherein the redirection memory comprises a programmable table storing associations between line cards serviced by the switch and the routing parameter sets in the routing memory for the switch.

20. A system for associating router parameters for a switch with line cards serviced by the switch, comprising:

a computer-readable medium; and

software stored on the computer-readable medium, the software operable to initially associate a router parameter set in a router memory for a switch with a first line card, the router parameter set including a plurality of routing parameters to be provided to the switch to service the first line card, and, in response to an event initiating activation of a second line card in place of the first line card, to reassociate the router parameter set with a second line card.

21. The system of Claim 20, wherein the event comprises failure of the first line card.

22. The system of Claim 20, the software further operable to initially associate a second set in the router memory with the second line card, the second router set including a plurality of router parameters to be provided to the switch to service the second line card, and, in response to the event, to reassociate the second router parameter set with the first line card.

23. The system of Claim 20, wherein the routing parameters comprise instructions, the routing parameter set comprises an instruction set and the routing memory comprises an instruction memory.

24. The system of Claim 23, wherein the switch comprises a synchronous switch.

25. The system of Claim 24, wherein the synchronous switch is a time slot interchanger (TSI).

26. A synchronous switch for a telecommunications node, comprising:

a time slot interchanger (TSI) operable to switch traffic between time slots for a plurality of line cards;

an instruction memory for the TSI, the instruction memory comprising a plurality of instruction sets, each instruction set including a plurality of instructions operable to be provided to the TSI to switch time slots of an associated line card;

a redirection memory operable to selectively associate each instruction set of the instruction memory with a disparate one of the line cards; and

a controller operable to reprogram the redirection memory to change associations of the instruction sets with the line cards.

27. The synchronous switch of Claim 26 further comprising:

the redirection memory programmed to associate a first instruction set with a working line card and a second instruction set with a protect line card; and

the controller operable to reprogram the redirection memory to associate the first instruction set with the protect line card and the second instruction set with the working line card in response to failure of the first line card and activation of the second line card in place of the first line card.

28. A system for associating routing parameters for a switch with line cards serviced by the switch, comprising:

means for programming a redirection memory to associate a routing parameter set in a routing memory for a switch with a first line card, the routing parameter set including a plurality of parameters to be provided to the switch to service the first line card; and

means for reprogramming the redirection memory to associate the routing parameter set in the routing memory with the second line card in response to an event initiating activation of a second line card in place of the first line card.

29. The system of Claim 28, wherein the event is a failure of a first line card.

30. The system of Claim 28, further comprising:

means for programming the redirection memory to associate a second routing parameter set in the routing memory with the second line card, the second routing parameter set including a plurality of routing parameters to be provided to the switch to service the second line card; and

means for reprogramming the redirection memory to associate the second routing parameter set with the first line card in response to the event initiating activation of the second line card in place of the first line card.

METHOD AND SYSTEM FOR REPROGRAMMING INSTRUCTIONS FOR A SWITCH

ABSTRACT OF THE DISCLOSURE

The method and system for reprogramming instructions for a switch includes programming a redirection memory to associate a routing parameter set in a routing memory for the switch with a first line card. The routing parameter set includes a plurality of routing parameters to be provided to the switch to service the first line card. In response to an event initiating activation of a second line card in place of the first line card, the redirection memory is reprogrammed to associate the routing parameters set in the routing memory with the second line card.

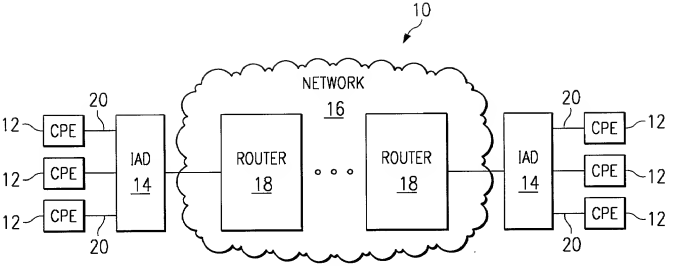

FIG. 1

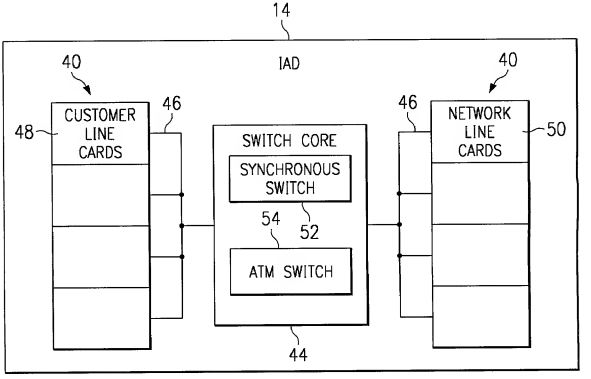

FIG. 2

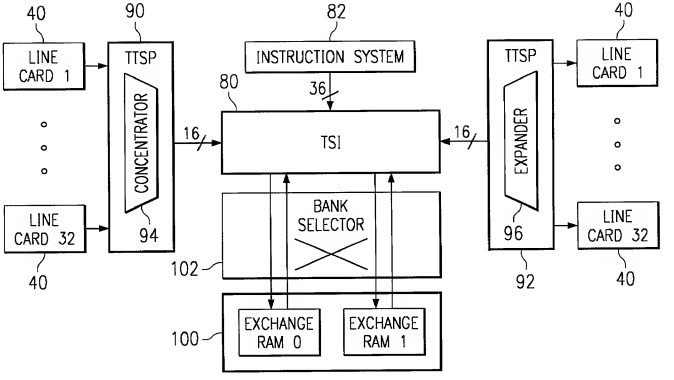

FIG. 3

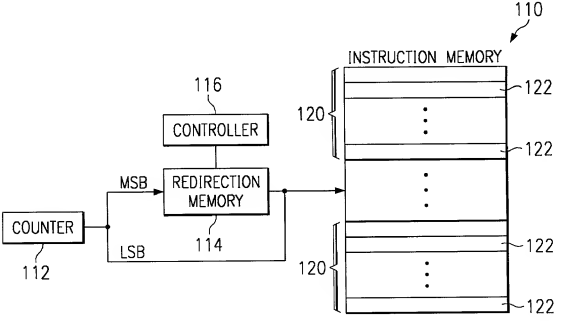

FIG. 4

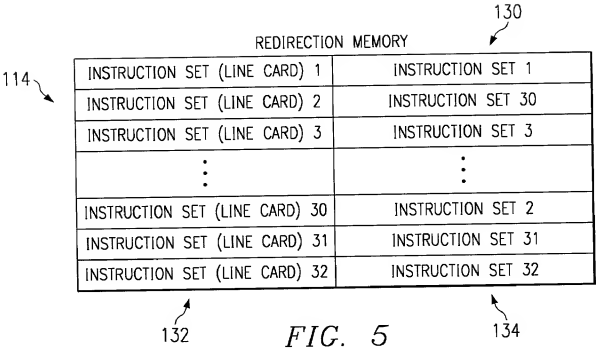

FIG. 5

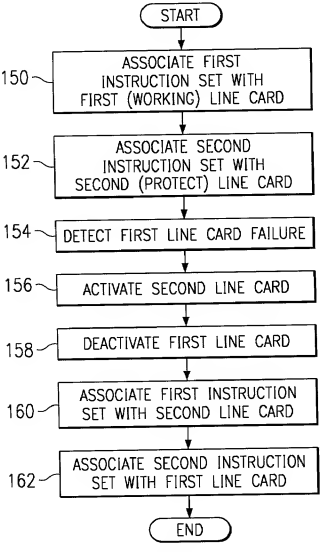

FIG. 6

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; that I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention or design entitled METHOD AND SYSTEM FOR REPROGRAMMING INSTRUCTIONS FOR A SWITCH, the specification of which (check one):

__X__ is attached hereto; or

_____ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable);

that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above; and that I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application(s) for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Number	Country	Date Filed	Priority Claimed (Yes) (No)
----------NONE----------			

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application(s) in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Serial Number	Date Filed	Status
----------NONE----------		

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all of the firm of Baker Botts L.L.P., my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith and to file and prosecute any international patent applications filed thereon before any international authorities under the Patent Cooperation Treaty.

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I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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